Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CX1**
2. **RX1**
3. **N.CD1**
4. **I1**
5. **N.I0**
6. **Q1**
7. **N.Q1**
8. **GND**
9. **N.Q2**
10. **Q2**
11. **N.I0**
12. **I1**
13. **N.CD2**
14. **RX2**
15. **CX2**
16. **VCC**

**.064”**

**.068”**

**5 4 3 2**

**6**

**7**

**8**

**9**

**10**

**11 12 13 14**

**1**

**16**

**15**

**B**

**6**

**0**

**2**

**Z**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: B602 Z**

**APPROVED BY: DK DIE SIZE .064” X .068” DATE: 1/24/23**

**MFG: NSC / FCH THICKNESS .014” P/N: 96L02**

**DG 10.1.2**

#### Rev B, 7/19/02